aforementioned embodiments of the present invention, the bump 3 can be directly connected to the electrode 5 by being pressed against the electrode 5 of the circuit board 4 with a load (for example, a pressure force of not smaller than 20 gf per bump 3) heavier than in the first and second prior art examples without being leveled in the leveling process as an independent process. Therefore, the connection resistance value does not depend on the number of interposed particles, and the connection resistance value can be stably obtained.

Although the conventional leveling process has been performed in order to shape the bump height constant at the time of bonding to the board electrode, the crushing of the bumps 3 can be performed concurrently with the bonding to the electrodes 2 or 5 in each of the embodiments of the present invention. Therefore, no independent leveling process is needed, and the bonding can be achieved while correcting the warp and undulation of the circuit board 4 by deforming the same, or the bonding is achieved while correcting the warp and undulation of the circuit board 4 by deforming the same without the need for the leveling process of the bumps 3 and 103 by hardening the conductive paste stuck to the bumps 3 and 103 and deforming the conductive paste at the time of bonding. Accordingly, this arrangement tolerates the warp and undulation.

There are needed a high-accuracy board 4 and the leveling of the bumps 3 and 103, as exemplified by 10 μm per IC chip (meaning that a thickness warp dimension accuracy of 10 μm per IC chip is needed) in the first prior art, 2 μm per IC chip in the second prior art, and 1 μm per IC chip in the third prior art (bump height variation of not greater than ± 1 μm). In practice, a glass board represented by LCD is employed. In contrast to this, according to the aforementioned embodiments of the present invention, the bonding is achieved while correcting the warp and undulation of the circuit board 4 by deforming the same at the time of bonding. Therefore, a board of a degraded surface flatness including warp and undulation, exemplified by a resin board, a flexible board, a multilayer ceramic board, or the like, can be employed, and a less expensive versatile IC chip bonding method can be provided.

If the volume of the thermosetting resin 306m located between the IC chip 1 and the circuit board 4 is set greater than the volume of the space between the IC chip 1 and the circuit board 4, then the resin flows out of this space, producing the encapsulating effect. Therefore, it is not required to lay an encapsulation resin (underfill coat) under the IC chip after the bonding of the IC chip to the circuit board with the conductive adhesive, which has

been needed in the first prior art, and the process can be shortened.

By mixing the inorganic filler 6f with the thermosetting resin 306m by about 5 to 90 wt% of the thermosetting resin 306m, the elastic modulus and the coefficient of thermal expansion of the thermosetting resin can be controlled to be optimum for the board 4. In addition to this, if this is utilized for the ordinary plating bump, then the inorganic filler enters the space between the bump and the circuit board, degrading the bonding reliability. However, if the stud bump (forming method utilizing wire bonding) is employed as in the aforementioned embodiments of the present invention, then the inorganic filler 6f and also the thermosetting resin 306m are forced outwardly of the bumps 3 and 103 by the pointed bumps 3 and 103 that enter the thermosetting resin 306m at the beginning of the bonding. By this operation, the inorganic filler 6f and the thermosetting resin 306m are forced outwardly of the space between the bumps 3 and 103 and the electrodes 5 and 2 in the process of the deformation of the pointed bumps 3 and 103, and the unnecessary interposed object can be eliminated, allowing the reliability to be further improved.

According to the present invention described above, the method and apparatus for bonding electronic